PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Mirmajid Seyyedy

Serial No.: 09/911,116

Filed: July 23, 2001

For: FLIP CHIP TECHNIQUE FOR CHIP ASSEMBLY

Examiner: David E. Graybill

Group Art Unit: 2827

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95-1024.3)

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Amanda Holland
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AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This amendment is in response to the Office Action of August 14, 2002, whose initial period of response is set to expire on November 14, 2002.

IN THE SPECIFICATION:

Please note that paragraph **[0001]**, is shown below, in clean form, for clarity.

[0001] Cross Reference to Related Applications: This application is a continuation of application Serial No. 09/392,153, filed September 8, 1999, now U.S. Patent 6,265,775 B1, issued July 24, 2001, which is a divisional of application Serial No. 08/788,209, filed January 24, 1997, now U.S. Patent 6,221,753 B1, issued April 24, 2001.

IN THE CLAIMS:

Cancel claims 3, 10, 14, and 18.

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

1. (Twice Amended) An assembly comprising:

a first semiconductor die having at least one lead on an active surface thereof, said at least one lead having at least one conductive pad disposed thereon, said at least one conductive pad having an upper surface, having a thickness and extending above said active surface of said first semiconductor die said thickness of said at least one conductive pad, said semiconductor die substrate having a passivation layer disposed on said active surface thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via, and said first semiconductor die having a layer of adhesive covering at least a portion of said passivation layer on said active surface, said layer of adhesive having a thickness; and

a substrate having at least one lead on a facing surface thereof, said at least one lead of said substrate having at least one conductive pad disposed thereon, said at least one conductive pad of said substrate having an upper surface, having a thickness and extending above said facing surface of said substrate, said thickness of said at least one conductive pad of said substrate being at least a combined thickness of said layer of adhesive covering at least a portion of said passivation layer on said active surface of said first semiconductor die and a remaining portion of said at least one via having said at least one conductive pad of said first semiconductor die extending thereinto; said

substrate being attached to said first semiconductor die by said adhesive layer of said first semiconductor die, said first semiconductor die having said upper surface of said at least one conductive pad on said at least one lead substantially forming movable, electrical contact without mechanical attachment with said upper surface of said at least one conductive pad on said at least one lead of said substrate, said movable electrical contact provided when said second substrate die is permanently attached to said first semiconductor die by said layer of adhesive.

2. (Twice Amended) The assembly of claim 1, wherein at least one of said active surface of said first semiconductor die and said facing surface of said substrate includes at least one groove thereon.

4. (Twice Amended) The assembly of claim 1, wherein at least one of said first semiconductor die and said substrate comprises a silicon wafer.

5. (Twice Amended) An assembly comprising:

a first semiconductor die having at least one lead on an active surface thereof, said at least one lead having at least one conductive pad disposed thereon, said at least one conductive pad having an upper surface, having a thickness and extending above said active surface of said first semiconductor die said thickness of said at least one conductive pad, said first substrate having a passivation layer disposed on said active surface thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via; and

a substrate having at least one lead on a facing surface thereof, said at least one lead of said substrate having at least one conductive pad disposed thereon, said at least one conductive pad of said substrate having an upper surface, having a thickness and

extending above said facing surface of said second substrate, said thickness of said at least one conductive pad of said substrate being at least a thickness of a remaining portion of said at least one via having said at least one conductive pad of said first semiconductor die extending thereinto, said first semiconductor die being attached to said substrate by an encapsulation material substantially surrounding said first semiconductor and a portion of said substrate, said first substrate having said upper surface of said at least one conductive pad on said at least one lead of said first semiconductor die substantially forming movable, electrical contact without mechanical attachment with said upper surface of said at least one conductive pad on said at least one lead of said substrate.

6. (Twice Amended) An assembly comprising:

a semiconductor wafer device having at least one lead on a first side thereof, said at least one lead having at least one conductive pad disposed thereon having a substantially flat surface thereon, having a thickness and extending above said first side of said semiconductor wafer device said thickness of said at least one conductive pad, said semiconductor wafer device having a passivation layer disposed on said first side thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via, and said semiconductor wafer device having a layer of adhesive covering at least a portion of said passivation layer on said first side, said layer of adhesive having a thickness; and

at least one semiconductor die having at least one lead on a first side thereof, said at least one lead of said semiconductor die having at least one conductive pad disposed thereon, said at least one conductive pad of said semiconductor die having a substantially flat surface thereon, having a thickness and extending above said first side of said semiconductor die, said thickness of said at least one conductive pad of said semiconductor die being at least a combined thickness of said layer of adhesive covering said at least a portion of said

passivation layer on said first side of said semiconductor wafer device and a remaining portion of said at least one via having said at least one conductive pad of said semiconductor wafer device extending thereinto, said semiconductor wafer device being juxtaposed to said first semiconductor die by said layer of adhesive, said semiconductor wafer device having said substantially flat surface of said at least one conductive pad on said at least one lead of said semiconductor wafer device forming movable, electrical contact without mechanical attachment with said substantially flat surface of said at least one conductive pad on said at least one lead of said semiconductor die, said movable, electrical contact provided when said semiconductor wafer device is permanently juxtaposed to said semiconductor die by said layer of adhesive.

7. (Twice Amended) A semiconductor assembly comprising:

a first semiconductor substrate having at least one lead on a facing surface thereof, said at least one lead having at least one conductive pad disposed thereon, said at least one conductive pad having an upper surface, having a thickness and extending above said facing surface of said first substrate said thickness of said at least one conductive pad, said first substrate having a passivation layer disposed on said facing surface thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via; and

a second semiconductor substrate having at least one lead on a facing surface thereof, said at least one lead of said second substrate having at least one conductive pad disposed thereon, said at least one conductive pad of said second substrate having an upper surface, having a thickness and extending above said facing surface of said second substrate, said thickness of said at least one conductive pad of said second substrate being at least a thickness of a remaining portion of said at least one via having said at least one conductive pad of said first substrate extending thereinto, one of said first substrate and

said second substrate being attached to another one of said first substrate and said second substrate by a glob top covering said one of said first substrate and said second substrate and adhering to at least a portion of said facing surface of said another one of said first substrate and said second substrate, said one of said first substrate and said second substrate having said upper surface of said at least one conductive pad on said at least one lead thereof substantially forming movable, electrical contact without mechanical attachment with said upper surface of said at least one conductive pad on said at least one lead of said another one of said first substrate and said second substrate, said movable, electrical contact provided when said one of said first substrate and said second substrate is permanently attached to said another one of said first substrate and said second substrate by said glob top.

8. (Twice Amended) A semiconductor assembly comprising:

a first semiconductor device having at least one lead on a first side thereof, said at least one lead having at least one conductive pad disposed thereon having a substantially flat surface thereon, having a thickness and extending above said first side of said first semiconductor device said thickness of said at least one conductive pad, said first semiconductor device having a passivation layer disposed on said first side thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via; and

a second semiconductor device having at least one lead on a first side thereof, said at least one lead of said second semiconductor device having at least one conductive pad disposed thereon, said at least one conductive pad of said second semiconductor device having a substantially flat surface thereon, having a thickness and extending above said first side of said second semiconductor device, said thickness of said at least one conductive pad of said second semiconductor device being at least a thickness of a remaining portion of said at least one via having said at least one conductive pad of said first semiconductor device extending thereinto, said second semiconductor device being juxtaposed to said first semiconductor device with said substantially flat surface of said at least one conductive pad on said at least one lead of said first semiconductor device substantially movably electrically contacting without mechanical attachment said substantially flat surface of said at least one conductive pad on said at least one lead of said second semiconductor device substantially making electrical contact therewith, said first semiconductor device being attached to said second semiconductor device by an encapsulation material substantially surrounding said first semiconductor device and a portion of said second semiconductor device.

9. (Previously Amended) The semiconductor assembly of claim 8, wherein at least one of said first side of said first semiconductor device and said first side of said second semiconductor device includes at least one groove thereon.

11. (Previously Amended) The semiconductor assembly of claim 9, wherein at least one of said first semiconductor device and said second semiconductor device comprises a silicon wafer.

12. (Previously Amended) An assembly comprising:

a first semiconductor device having a plurality of leads on a first side thereof, each lead of said plurality of leads having a conductive pad disposed thereon in a substantially horizontal plane, each conductive pad having a substantially flat surface disposed in said substantially horizontal plane thereon, having a thickness and extending above said first side of said first semiconductor device said thickness of said each conductive pad, said first semiconductor device having a passivation layer disposed on said first side thereof having a thickness greater than said thickness of said each conductive pad, said passivation layer having at least one via therein for said each conductive pad, said each conductive pad extending into and through only a portion of said at least one via, and said first semiconductor device having a layer of adhesive covering at least a portion of said passivation layer on said first side, said layer of adhesive having a thickness; and

a second semiconductor device having a plurality of leads on a first side thereof, each lead of said plurality of leads of said second semiconductor device having a conductive pad disposed thereon in a substantially horizontal plane, each conductive pad of said second semiconductor device having a substantially flat surface disposed in said substantially horizontal plane thereon, having a thickness and extending above said first side of said second semiconductor device, said thickness of said each conductive pad of said second semiconductor device being at least a combined thickness of said layer of adhesive covering at least a portion of said passivation layer on said first side of said first semiconductor device and a remaining portion of said each at least one via having said conductive pad of said first semiconductor device extending thereinto, said second semiconductor device being juxtaposed to said first semiconductor device by said layer of adhesive, said first semiconductor device having at least one conductive pad disposed on at least one lead of said plurality of leads of said first semiconductor device forming movable electrical contact without mechanical attachment with at least one conductive pad on at least one lead of said plurality of leads of said second semiconductor device,

said movable, electrical contact provided when said second semiconductor device is permanently attached to said first semiconductor device by said layer of adhesive.

13. (Previously Amended) The assembly of claim 12, wherein at least one of said first side of said first semiconductor device and said first side of said second semiconductor device includes at least one groove thereon.

15. (Previously Amended) The assembly of claim 12, wherein at least one of said first semiconductor device and said second semiconductor device comprises a silicon wafer.

16. (Twice Amended) An assembly comprising:

a silicon substrate having a plurality of leads on a first side thereof, each lead of said plurality of leads having a conductive pad disposed thereon in a substantially horizontal plane, each conductive pad having a substantially flat surface disposed in said substantially horizontal plane thereon, having a thickness and extending above said first side of said silicon substrate said thickness of said each conductive pad, said silicon substrate having a passivation layer disposed on said first side thereof having a thickness greater than said thickness of said each conductive pad, said passivation layer having at least one via therein for said each said conductive pad, said each conductive pad extending into and through only a portion of said at least one via, and said silicon substrate having a layer of adhesive covering at least a portion of said passivation layer on said first side, said layer of adhesive having a thickness; and at least two semiconductor devices, each having a plurality of leads on a first side thereof, each lead of said plurality of leads having a conductive pad disposed thereon in a substantially horizontal plane, each conductive pad having a substantially flat surface disposed in said substantially horizontal plane thereon, having a thickness and extending above said first side of a semiconductor device, said thickness of said each conductive pad of a semiconductor device being at least a

combined thickness of said layer of adhesive covering at least a portion of said passivation layer on said first side of said silicon substrate and a remaining portion of said each at least one via having said each conductive pad of said silicon substrate extending thereinto, said at least two semiconductor devices being juxtaposed to said silicon substrate by said layer of adhesive, said silicon substrate having said conductive pad on at least one lead of said plurality of leads on said silicon substrate forming movable electrical contact without mechanical attachment with said conductive pad on at least one lead of said plurality of leads of a semiconductor device, said movable, electrical contact provided when a semiconductor device is permanently attached to said silicon substrate by said layer of adhesive.

17. (Twice Amended) The assembly of claim 16, wherein at least one of said first side of said silicon substrate and said first side of a semiconductor device includes at least one groove thereon.

19. (Twice Amended) The assembly of claim 16, wherein at least one of said silicon substrate and a semiconductor device comprises a silicon wafer.

20. (Twice Amended) An assembly comprising:

a substrate having at least one lead on a facing surface thereof, said at least one lead having at least one conductive pad disposed thereon, said at least one conductive pad having an upper surface, having a thickness and extending above said facing surface of said substrate said thickness of said at least one conductive pad, said substrate having a passivation layer disposed on said facing surface thereof having a thickness greater than said thickness of said at least one conductive pad, said passivation layer having at least one via therein, said at least one conductive pad extending into and through only a portion of said at least one via; and

at least one silicon semiconductor device having at least one lead on an active surface thereof having at least one bond pad disposed thereon, said at least one bond pad of said at least one silicon semiconductor device having an upper surface, having a thickness and extending above said active surface of said at least one silicon semiconductor device, said at least one silicon semiconductor device having a layer of adhesive having a thickness on at least a portion of said active surface thereof, said at least one silicon semiconductor device being attached to said substrate by said layer of adhesive, said upper surface of said at least one conductive pad on said at least one lead of said substrate substantially forming movable, electrical contact without mechanical attachment with said upper surface of said at least one bond pad on said at least one lead of said at least one silicon semiconductor device, said movable electrical contact provided when said at least one silicon semiconductor device is permanently attached to said substrate by said layer of adhesive.

REMARKS

Claims 1, 2, 4 through 9, 11 through 13, 15 through 17, 19 and 20 are currently pending in the application.

Claims 3, 10, 14, and 18 have been canceled.

This amendment is in response to the Office Action of August 14, 2002.

Claims 1, 3, 5 through 8, 10, 12, 14, 16 through 18 and 20 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 4, 10, 14 and 18 of prior United States Patent 6,265,775 (hereinafter referred to as the `775 patent). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant submits that a reliable test for double patenting under 35 U.S.C. § 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. Is there an embodiment of one invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting under 35 U.S.C. § 101 does not exist. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

In the present application, Applicant submits that different embodiments of the presently claimed invention of independent claims 1, 5, 6, 7, 8, 12, 16, and 20 are being claimed than in corresponding claims of the `775 patent. For instance, presently amended independent claim 1 of the present application is directed to "An assembly comprising . . . a first semiconductor die . . . and a substrate . . . . In contrast, at best, the claimed invention of independent claim 1 and dependent claim 4 therefrom of the `775 patent are directed to "A semiconductor assembly . . .a first substrate . . . and a second substrate . . . ." wherein one of the first substrate and the second substrate comprises a flip chip. Clearly, a different embodiment of the invention is being claimed in presently amended independent claim 1 of the present application of an assembly and the semiconductor assembly of the `775 patent as an assembly is not the same as a semiconductor assembly and a flip chip type semiconductor die is not the same

embodiment of the invention as a semiconductor die. Accordingly, presently amended claim 1 is allowable 6 is allowable as the identical invention is not being claimed under 35 U.S.C. § 101.

Similarly, presently amended independent claim 5 of the present application is directed to "An assembly comprising . . . a first semiconductor die . . . and a substrate . . . ." Whereas the embodiment of the invention claimed in independent claim 1 and dependent claim 5 of the `775 patent is directed to . "A semiconductor assembly . . .a first substrate . . . and a second substrate . . . ." wherein one of the first substrate and the second substrate comprises a silicon wafer. Clearly, a different embodiment of the invention is being claimed in presently amended independent claim 5 of the present application of an assembly and the semiconductor assembly of the `775 patent as an assembly is not the same as a semiconductor assembly and a silicon wafer is not the same embodiment of the invention as a semiconductor die or a substrate. Accordingly, presently amended claim 5 is allowable 6 is allowable as an identical embodiment of the invention is not being claimed under 35 U.S.C. § 101.

Additionally, presently amended independent claim 5 of the present application is directed to "An assembly comprising . . . a semiconductor wafer device . . . and at least one semiconductor die . . . . In contrast, at best, the claimed invention of independent claim 6 of the `775 patent is directed to a semiconductor assembly comprising a first substrate and a second substrate, not the embodiment of the invention of presently amended independent claim 6. Clearly, an assembly is a different embodiment of the invention than a semiconductor assembly as well as a semiconductor wafer device and a semiconductor die is a different embodiment of the invention than a first substrate and a second substrate, even if one of them is a flip chip. Accordingly, presently amended independent claim 6 is allowable as an identical embodiment of the invention is not being claimed under 35 U.S.C. § 101.

Applicant further submits that the embodiment of the invention set forth in presently amended independent claim 7 is not the identical embodiment of the invention set forth in independent claim 7 of the `775 patent as a first semiconductor substrate and a second

semiconductor substrate are not identical to a first substrate and a second substrate. Accordingly, claim 7 is allowable as no double patenting under 35 U.S.C. § 101 is present.

Turing to presently amended independent claim 8, Applicant submits that the embodiment of the invention set forth in presently amended independent claim 8 is not the identical embodiment of the invention set forth in independent claim 8 of the `775 patent as a first semiconductor device and a second semiconductor device are not identical to a first substrate and a second substrate. Accordingly, claim 8 is allowable as no double patenting under 35 U.S.C. § 101 is present.

Considering presently amended independent claim 12, Applicant submits that the embodiment of the invention set forth in independent claim 12 is not the identical embodiment of the invention set forth in independent claim 12 of the `775 patent as a first semiconductor device and a second semiconductor device are not identical to a first substrate and a second substrate. Accordingly, claim 12 is allowable as no double patenting under 35 U.S.C. § 101 is present.

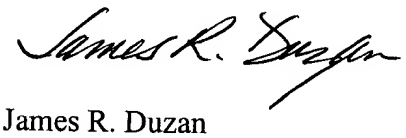
Applicant submits that the embodiment of the invention set forth in presently amended independent claim 16 is not the identical embodiment of the invention set forth in independent claim 16 of the `775 patent as a silicon substrate and at least two semiconductor devices are not identical to a first silicon substrate and a second silicon substrate. Accordingly, claim 8 is allowable as no double patenting under 35 U.S.C. § 101 is present.

Finally, Applicant submits that the embodiment of the invention set forth in presently amended independent claim 20 is not the identical embodiment of the invention set forth in independent claim 20 of the `775 patent as a substrate and at least one silicon semiconductor device are not identical to a first substrate and a second substrate. Accordingly, claim 20 is allowable as no double patenting under 35 U.S.C. § 101 is present.

Applicant submits that claims 1, 2, 4 through 9, 11 through 13, 15 through 17, 19 and 20 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1, 2, 4 through 9, 11 through 13, 15 through 17, 19 and 20 and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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